What is claimed is:

1. A diode circuit comprising
at least three contacts, wherein one contact is connected to a region of a first polarity and the other at least two contacts are connected to regions of the opposite polarity and are separated from each other by a partially resistive region.

2. A diode of claim1, wherein the partially resistive region is a well region.

3. A diode of claim 2, wherein the diode is a p-well diode and is provided with a cathode contact connected to a n+ region and two or more anode contacts connected to p+ regions.

4. A diode of claim 2, wherein the diode is a n-well diode and is provided with an anode contact connected to a p+ region and two or more cathode contacts connected to n+ regions.

5. A diode circuit, comprising
three contacts providing a first current path between an anode and a cathode, and a second current path between a second anode or cathode and the first anode or cathode, respectively.

6. A diode comprising
a first region of a first polarity,
a first contact connected to the region of first polarity,
two regions of the opposite polarity to the first region, and
two second contacts each connected to one of the regions of the opposite polarity, wherein one of the two second contacts defines an input to the diode structure, while the other of the two second contacts defines an output of the diode structure.

7. A diode of claim 6, wherein the first region defines a cathode and the two regions of opposite polarity define anodes.

8. A diode of claim 6, wherein the first region defines an anode and the two regions of opposite polarity define cathodes.

9. A diode of claim 6, wherein the two regions of opposite polarity are separated by a partially resistive element.

10. A diode of claim 9, wherein the partially resistive element is a well region.

11. A method of reducing the voltage to which a protected circuit is exposed by a diode under ESD current pulses, comprising

using a first anode contact or cathode contact as an input to the diode structure, and

using a second contact to a region of the same polarity as the first contact as an output from the structure, wherein the second contact is separated from the first contact by a well region to provide a voltage drop between the contacts under ESD current pulse conditions.

12. An ESD protection circuit for an internal circuit that includes an I/O contact, comprising

an ESD clamp between power rails for the internal circuit,

a first diode structure between the I/O contact and one power rail, and

a second diode structure between a second power rail and the I/O contact, wherein each of the diode structures includes an input terminal providing contact to a region of a first polarity and connected to the I/O contact, and a separate output terminal providing contact to a second region of the first polarity and connected to the internal circuit.

13. An ESD protection circuit of claim 12, wherein the first and second regions input are separated by an internal resistive element of the diode structure.

14. An ESD protection circuit of claim 12, wherein the one diode structure is a p-well diode with a first anode terminal connected to the I/O contact and a second anode terminal connected to an input to the internal circuit and separated from the first anode terminal by a p-well, wherein a cathode terminal of said one diode structure is connected to a power rail, wherein the other diode structure is a n-well diode in which one cathode terminal is connected to the I/O contact and a second cathode terminal is connected to the input to the internal circuit and spaced from the first cathode by a n-well, and wherein an anode terminal of said other diode structure is connected to the other power rail.

15. An ESD protection circuit for protecting an input to an internal circuit from ESD current pulses to an I/O contact, comprising

a bipolar junction transistor structure for shunting current to ground, wherein the bipolar junction transistor structure includes a first base contact connected to the I/O contact, and a second base contact connected to the input of the internal circuit, wherein the two base contacts are separated by a resistive element between the two base contacts.

16. An ESD protection circuit of claim 15, wherein the resistive element includes a base polysilicon region.

17. A method of protecting an input to an internal circuit against ESD current pulses to an I/O contact, comprising

shunting the current pulse to ground by means of a bipolar junction transistor structure wherein the bipolar junction transistor structure includes a first base contact and a second base contact, and wherein the method includes connecting the first base contact to the I/O contact and the second base contact to the input of the internal circuit, and causing current flow to the first base contact to experience a voltage drop to the second base contact.

18. A method of claim 17, wherein the voltage drop between the first and second base contacts is achieved by directing current flow through at least one internal resistive element of the bipolar junction transistor structure.

19. A method of claim 18, wherein the internal resistive element includes a base polysilicon region to which both base contacts are connected.